

This diagram shows a cross-sectional view of a semiconductor device with two p+ regions. The left p+ region is labeled with a downward arrow and the label  $p^+$ . The right p+ region is labeled with an upward arrow and the label  $p^+$ . The device consists of a substrate (101) with a gate oxide layer (Gox) on top. The gate oxide layer is divided into two regions (102) by a central channel region (103). The channel region (103) is further divided into two sub-regions (103a) by a central barrier region (104). The barrier region (104) is shown with a dashed line, indicating it is a virtual barrier. The channel regions (103a) are shown with a diagonal hatching pattern. The gate oxide layer (Gox) is shown with a wavy line pattern. The substrate (101) is shown with a solid line pattern. The labels 101, 102, 103, 103a, 104, and Gox are used to identify the various components of the device.

FIG. 30A PRIOR ART

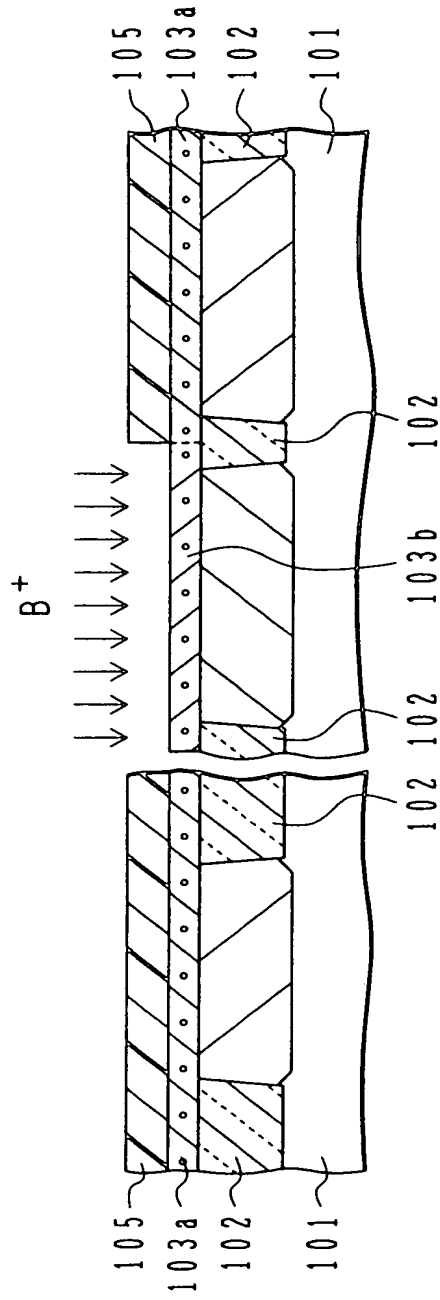
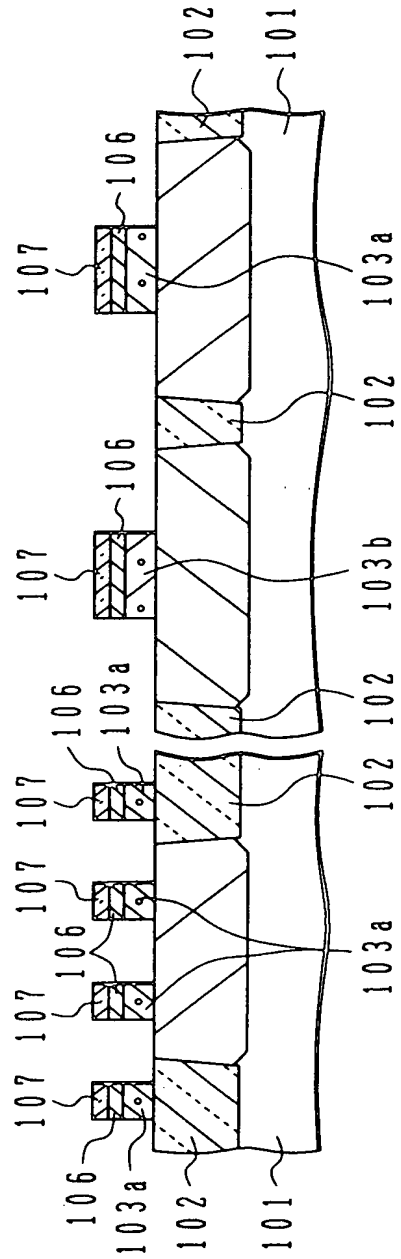
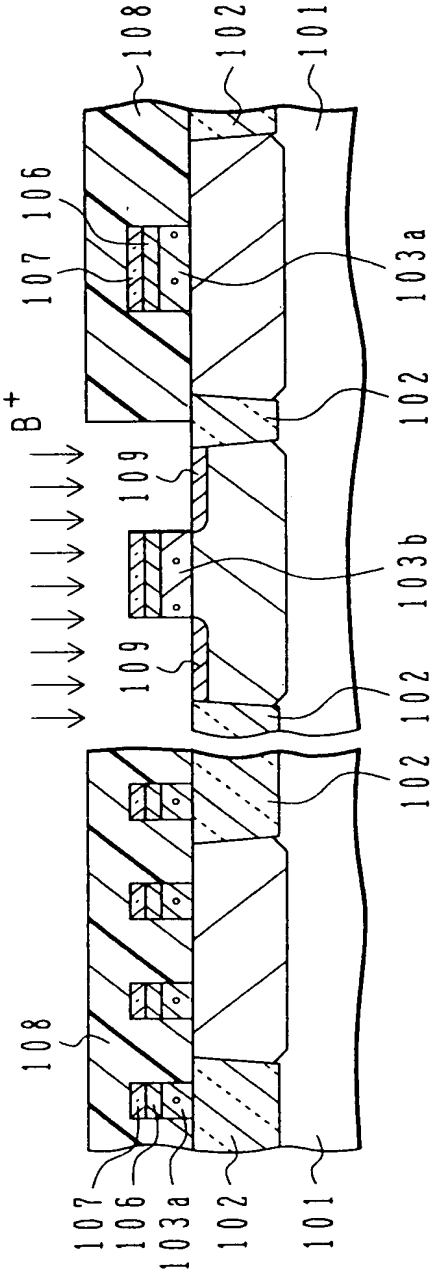


FIG. 30B PRIOR ART



**FIG. 31A** PRIOR ART



**FIG. 31B** PRIOR ART

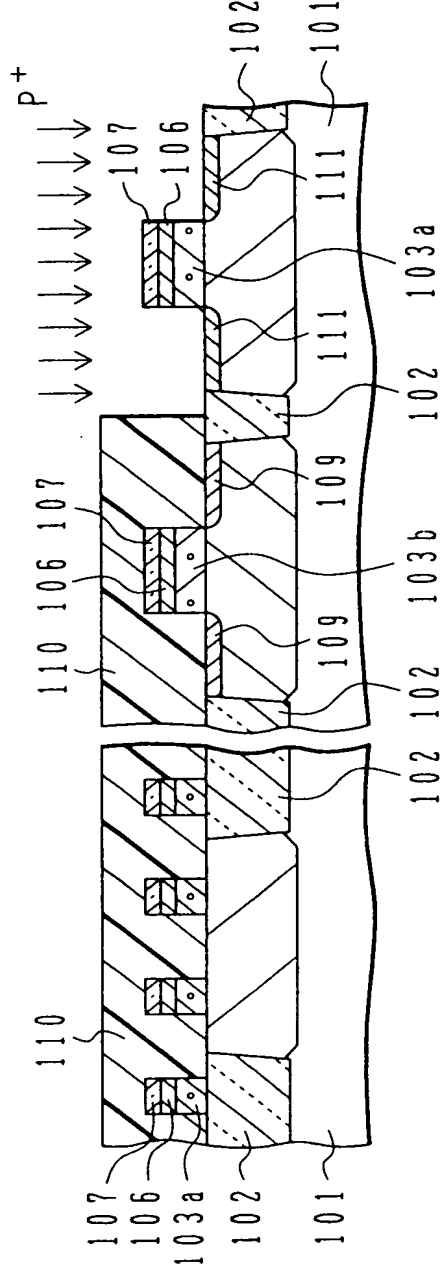


FIG. 32A PRIOR ART

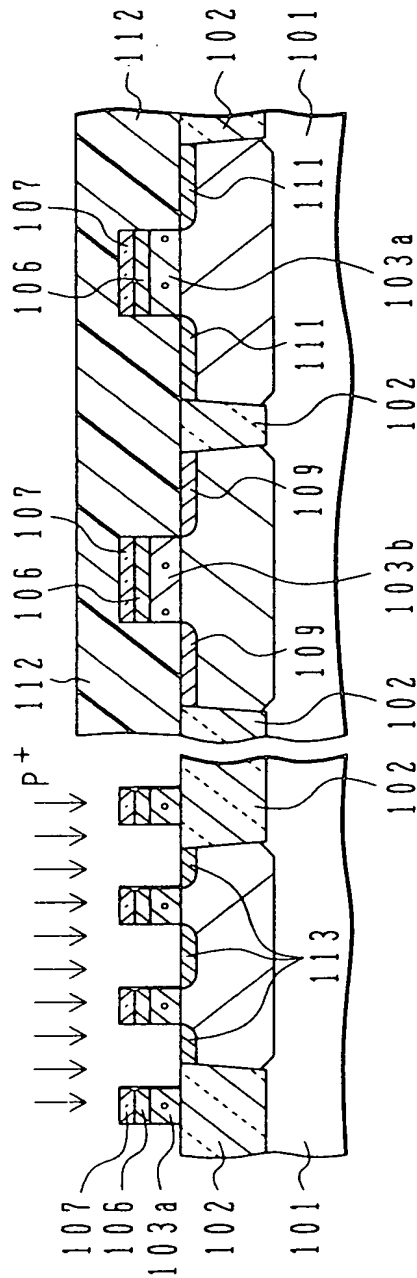
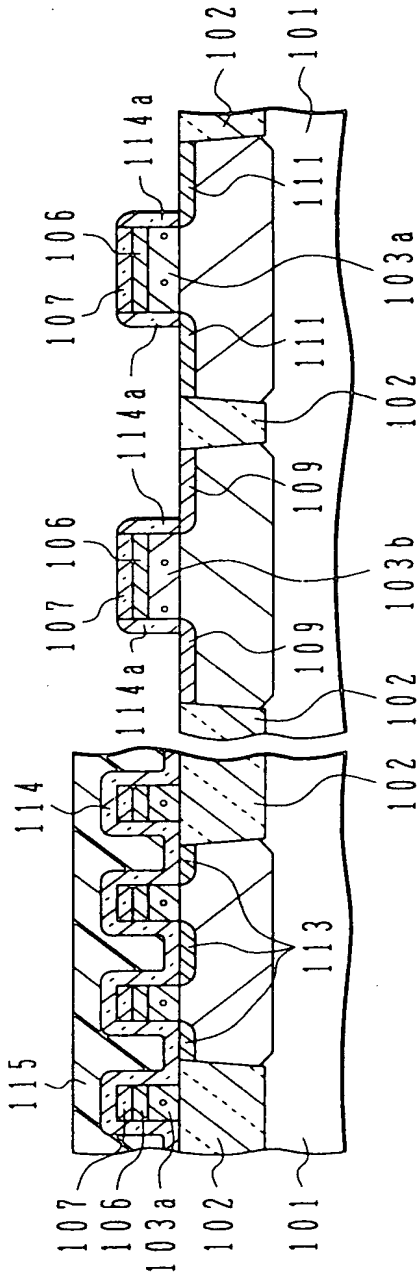
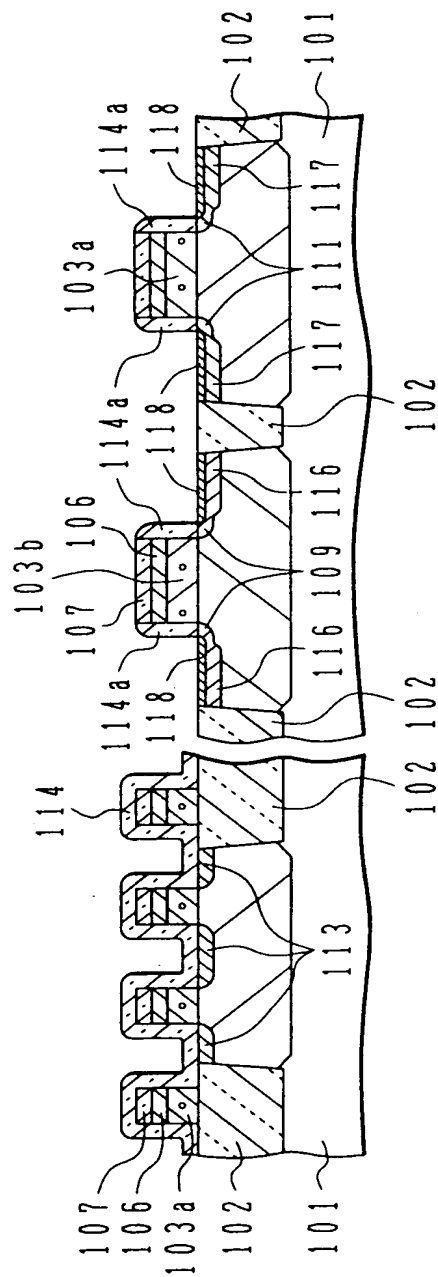


FIG. 32B PRIOR ART



**FIG.33** PRIOR ART



**FIG.34** PRIOR ART

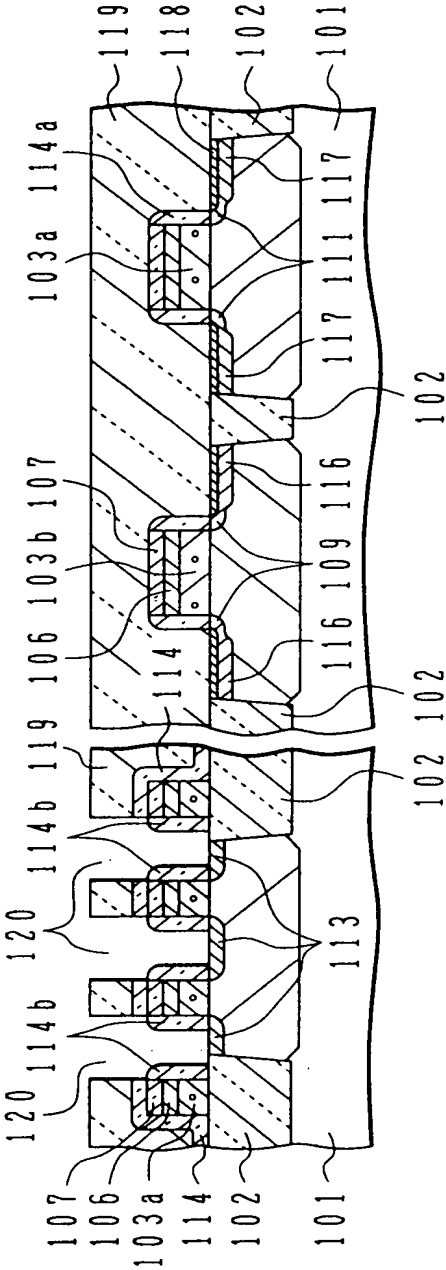
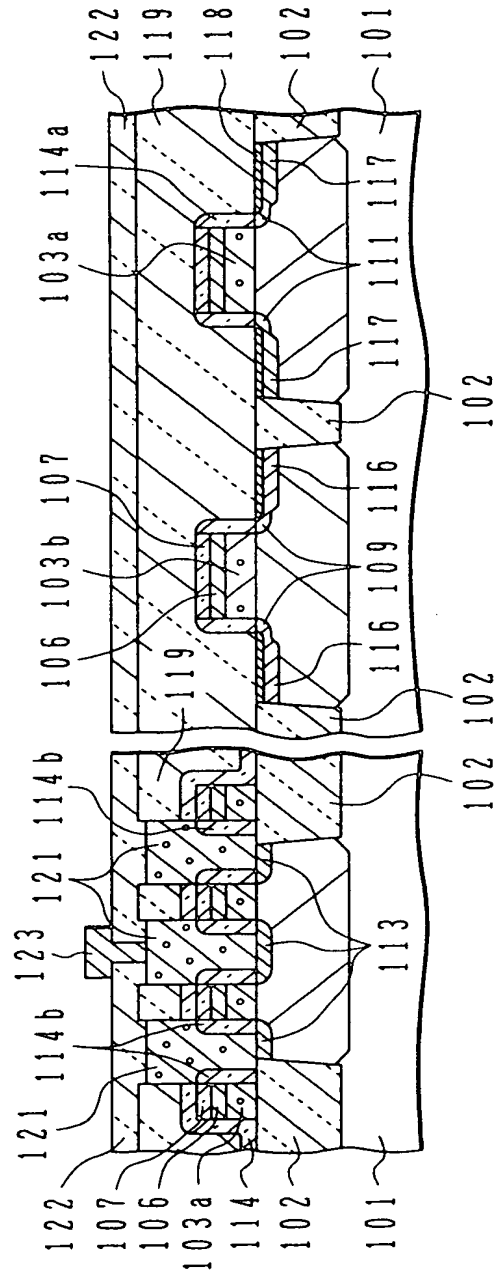


FIG. 35 PRIOR ART



**FIG.36** PRIOR ART

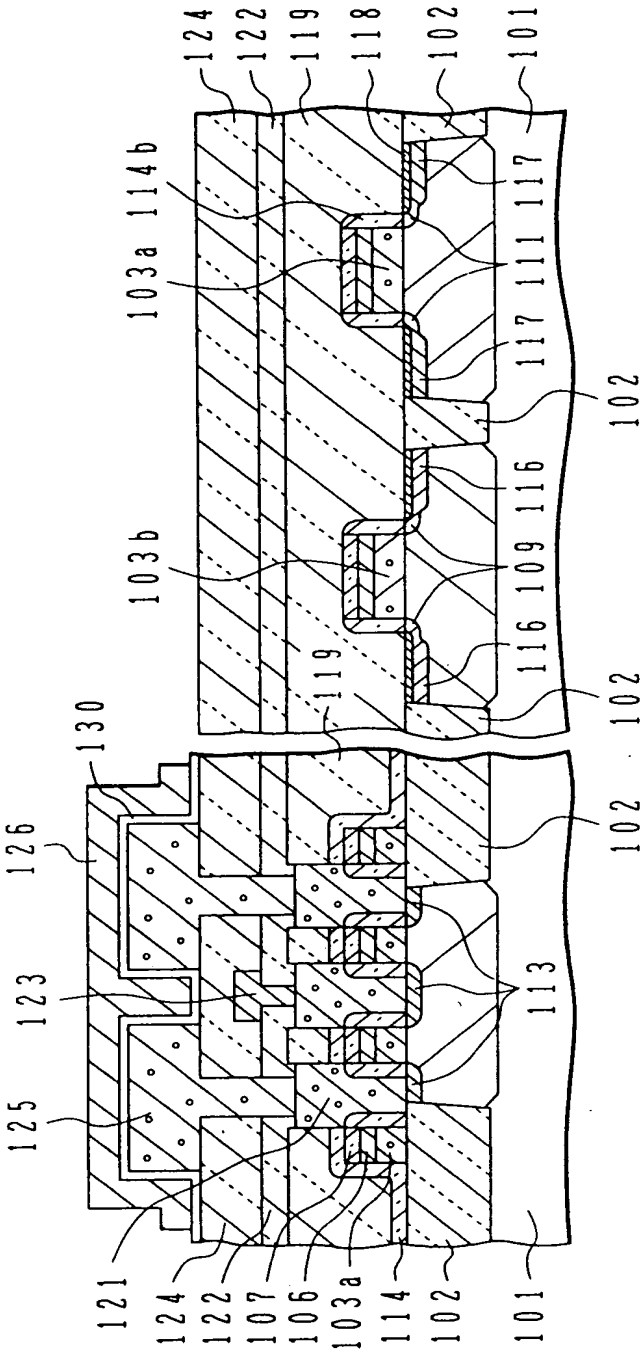
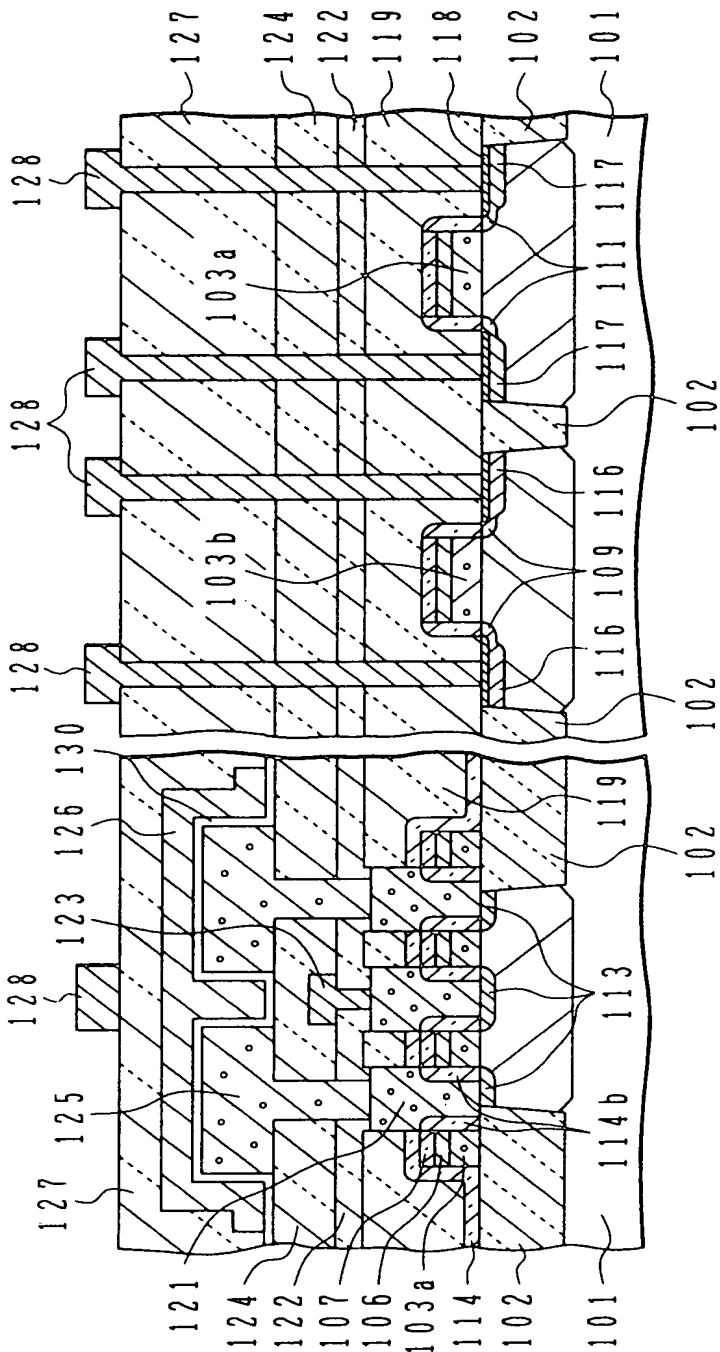




FIG. 37 PRIOR ART



**FIG.38** PRIOR ART

